REMARKS

SUMMARY:

The present application sets forth original claims 1-20, of which claims 1 and 12 are independent claims. Claims 21-41 stand previously cancelled.

Original claims 1, 3-5, and 8-11 stand rejected under 35 U.S.C §102(b) as being allegedly anticipated by U.S. Patent Nos. 4,811,162 (Maher et al.) or 6,232,144 (McLoughlin). Original claims 1-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,310,757 (Tuzuki et al.) in view of U.S. Patent No. 3,992,761 (McElroy et al.). Claims 2, 6, 7 and 12-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Maher et al. or McLoughlin in combination with Tuzuki et al.

Traversals of the prior art rejections summarized above are hereafter presented as well as comments with respect to requested amendments and to each individual argument presented by the Examiner.

BACKGROUND re PRESENTLY REQUESTED CLAIM AMENDMENTS:

Amendments to claims 1, 3-6, 8, 9, 12, and 14-17 are presented, without entry of any new matter, and otherwise intended as simply clarifications or other improvements on claim language per the Examiner's helpful comments, and not intended to result in any other substantive effect with respect to their scope.

For example, with respect to antecedent basis for use of terminology, the present application discusses various physical characteristics and features of subject matter variously discussed in the subject application in the context of constituting "structure" or "structures", including such recitations beginning as early as page two of the application, in the "Background" section, and reciting as follows on page 15 thereof, in the "Detailed Description" section: "The subject termination scheme utilizes exposed electrode portions of structures such as monolithic capacitor arrays, multilayer capacitors including those with interdigitated electrode configurations, integrated passive components, and other electronic chip structures."

Similarly, the present application throughout makes use of reference to present plating technology, including references in the context to "plating materials" (for example, page, 5, line 20 of the subject application), or "plating solution" (for example, page 22, lines 10-12 of the subject application: "...subjecting ... exposed electrode tabs to an electroless plating solution...."

In two respects, the Examiner in the subject Final Rejection (numbered page 5) alleges that two arguments previously made by Applicant with respect to independent claims 1 and 12 were not commensurate with the scope of the claims. Without intending to alter the scope of the claims, both independent claims 1 and 12 have been requested for amendment herewith, to clarify the claim language in such context.

Specifically, the Examiner noted with respect to the electroless bath that the claim language does not recite "entirely immersing" as would (allegedly) be commensurate with the scope of the submitted arguments. Applicants have included in both claims the terms "**fully** immersing" to clarify that the claim language and corresponding arguments are commensurate in scope. Applicants do not regard such requested amendment as a change in the scope of such claims because the claims likewise did not previously state "partially immersing." When considering the supporting disclosure, it is submitted that the prior language should have been interpreted as previously argued. However, to ensure a clarified claim recitation per the Examiner's interpretation of the claim language, the term "fully" is added herewith.

Likewise, the Examiner alleged that the "directly" depositing termination (plating) material nature of the claims previously argued was not supported by the claim language. Again, independent claim 1 is requested amended herewith, not with the intention of changing its scope, but to clarify that the plating material is deposited on selected of the **exposed** internal electrode elements. In the context of the present disclosure, it should be clear that such claimed "exposure" means that there is no intermediate coating. Independent claim 12 already includes reference to "respective bridged terminations among selected of the exposed internal electrode elements." The subject supporting disclosure therefore respectfully satisfies the context argued.

The dependent claims have been reviewed and revised regarding claim language solely for ensuring clarity and proper antecedent basis, in the contexts referenced above, and without entry of any new matter.

BACKGROUND CASE LAW RE 35 U.S.C. §102 & §103:

Before setting forth a discussion of the prior art patents applied in the recent Final Office Action, it is respectfully submitted that controlling case law has frequently addressed rejections under Sections 102 and Section 103.

"For a prior art reference to anticipate in terms of 35 U.S.C Section 102, every element of the claimed invention must be identically shown in a single reference." Diversitech Corp. v. Century Steps, Inc., 850 F.2d 675, 677, 7 U.S.P.Q.2d 1315, 1317 (Fed Cir, 1988; emphasis added). The disclosed elements must be arranged as in the claim under review. See Lindemann Machinefabrik v. American Hoist & Derrick Co., 730 F.2d 1452, 1458, 221 U.S.P.Q. 481, 485 (Fed. Cir. 1984). If any claim, element, or step is absent from the reference that is being relied upon, there is no anticipation. Kloster Speedsteel AB v. Crucible, Inc., 793 F.2d 1565, 230 U.S.P.Q. 81 (Fed. Cir. 1986). Anticipation under 35 U.S.C. Section 102 requires that there be an identity of invention. See Shatterproof Glass Corp. v. Libbey-Owens Ford Co., 758 F.2d 613, ___, 225 U.S.P.Q. 635, 637 (Fed. Cir. 1985). In PTO proceedings, claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. In re Sneed, 710 F.2d 1544, 1548, 218 U.S.P.Q. 385, 388 (Fed. Cir. 1983).

In addition to the well-known required multi-step analysis of Graham v. John Deere Co., 381 U.S. 1, 148 U.S.P.Q. 459 (S. Ct. 1966), and its progeny, the Court of Appeals for the Federal Circuit has on numerous occasions offered its guidance concerning the propriety of Section 103 rejections.

> Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined only if there is some suggestion or incentive to do so. (emphasis original)

ACS Hospital Systems, Inc. v. Montefiore Hospital, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984).

The task of the Patent Office is essentially a burden of proof not just to show prior patents with selected elements similar to respective parts of a claimed combination, but to show teachings to support obviously combining the elements in the manner claimed.

> Virtually all inventions are necessarily combinations of old elements. The notion, therefore, that combination claims can be declared invalid merely upon finding similar elements in separate prior patents would necessarily destroy virtually all patents and cannot be the law under the statute, ' 103. (footnotes omitted)

Panduit Corp. v. Dennison Manufacturing Co., 1 U.S.P.Q. 2d 1593, 1603 (Fed. Cir. 1987).

In In re Deminski, 230 U.S.P.Q. 313 (Fed. Cir. 1986), the court reversed a Patent Office Board of Appeals decision rejecting claims for obviousness, saying: "There [was] nothing in the prior art references, singly or in combination, 'to suggest the desirability, and thus the obviousness' of the [claimed subject matter]." Id. at 315; emphasis original. The court noted that the relied-on reference did not address the technical problem addressed by the claimed invention (and in fact taught away from the Applicant's invention), and stated the well-established principle that "[h]indsight analysis is clearly improper. . . ." Id. at 316.

In Bausch & Lomb v. Barnes-Hind/Hydrocurve, 230 U.S.P.Q. 416 (Fed. Cir. 1986), the court vacated a district court holding of invalidity for obviousness. In doing so, the district court was criticized for viewing teachings from the prior art in isolation, instead of considering the prior art references in their entirety; for entering the tempting but forbidden zone of hindsight analysis; for failing to view the claimed invention as a whole; and for disregarding express claim limitations. Id. at 419, 420.

> It is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts

> necessary to the full appreciation of what such reference fairly suggests to one skilled in the art. (citations omitted)

Bausch & Lomb v. Barnes-Hind/Hydrocurve, 230 U.S.P.Q. 416, 419 (Fed. Cir. 1986). (emphasis added)

> The Supreme Court in Graham and Adams . . . foreclosed the use of substitutes for facts in determining obviousness under section 103. The legal conclusion of obviousness must be supported by facts. [footnote omitted] Where the legal conclusion is not supported by facts, it cannot stand. . . .
>
> A rejection based on section 103 clearly must rest on a factual basis, and these facts must be interpreted without hindsight reconstruction of the invention from the prior art. . . . It [the Patent Office] may not, because it may doubt that the invention is patentable, resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis. . . .
>
> [W]e may not resolve doubts in favor of the Patent Office determination when there are deficiencies in the record as to the necessary factual bases supporting its legal conclusion of obviousness. (emphasis original)

In re Warner, 379 F.2d 1011, __, 154 U.S.P.Q. 173, 177, 178 (C.C.P.A. 1967).

Finally, the PTO Board of Appeals noted the following in Ex parte Clapp: "[S]implicity and hindsight are not proper criteria for resolving the issue of obviousness. " Ex parte Clapp, 227 U.S.P.Q. 972, 973 (PTO Bd. App. 1985).

REJECTION OF ORIGINAL CLAIMS 1, 3-5 AND 8-10 (35 U.S.C. §102(B)):

Original claims 1, 3-5 and 8-11 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Nos. 4,811,162 (Maher et al.) or 6,232,144 (McLoughlin). By rejecting original claims 1, 3-5 and 8-11 under 35 U.S.C. §102(b), an assertion is made by the Examiner that the Maher et al. and McLoughlin references disclose all the features of original independent claim 1, from which claims 3-5 and 8-11 variously depend.

As requested to be amended herewith, independent claim 1 sets forth a clarified method of forming electrolessly plated structures for electronic components, including a step of fully immersing a plurality of electronic components in an electroless plating bath solution for a predetermined amount of time such that a plating material is deposited on selected of exposed internal electrodes of the plurality of electronic component, and so that a termination structure is developed by controlled bridging of the plating material among selected of the exposed internal electrode elements. Both Maher et al. and McLoughlin references fail to disclose all such elements of presently clarified claim 1, and therefore as a matter of law respectfully cannot anticipate such amended independent claim 1.

Maher et al. discloses a capacitor end termination composition and related method of terminating such components. The multi-layered terminations formed in Maher et al. respectively include an initial base layer comprising a metallo organic resinate material. Such a base metal resinate acts as an adhesion promoter for facilitating the formation of a film on the surface on which the composition is applied (col. 2, lines 15-18). The silver based resinate is applied to a ceramic body at its ends by hand dipping or mechanically dipping the capacitor ends into the resinate composition (col. 3, lines 58-65). Only after formation of this initial layer may leach resistance boundary layers (e.g., nickel layers formed by electroplating or electrolytic plating) be formed thereon. There are many differences between the above terminations and related process steps as disclosed in Maher et al. versus clarified claim 1 as requested to be amended herewith.

Claim 1 as requested to be amended herewith for clarification sets forth that the subject plated structures (which are formed by depositing plating material directly on the electronic components) are formed by fully immersing a plurality of electronic components in an electroless plating bath solution. In contrast, the initial resinate termination layer of Maher et al. is formed by carefully dipping only the end portions of the capacitor chips in the resinate composition. If such termination material were applied according to the process of presently clarified claim 1, the resinate composition would cover the entire ceramic body, **shorting together all of the capacitor**

electrodes and destroying the functionality of the capacitors. Furthermore, such hand dipping or mechanical dipping process must be done on an individual component-by-component basis, not a bulk process as set forth in claim 1 as requested to be amended, whereby a plurality of electronic components are simultaneously terminated. The process set forth in clarified claim 1 as requested to be amended is much more time efficient and cost effective than that disclosed in Maher et al.

Thus, the initial resinate composition layer of the Maher et al. terminations cannot be the same as the plating referred to in claim 1 as presently requested to be amended. Further, the leach resistant boundary layer 16 disclosed in Maher et al. also cannot be compared to the plating referred to in such clarified claim 1. The boundary layer 16 disclosed in Maher et al. is not formed directly on the electronic components, but instead over the initial resinate termination layer, which is required for adhesion promotion of boundary layer 16. A fundamental aspect of the process set forth in clarified claim 1 as requested to be amended herewith is that the subject plated terminations are formed directly on the electronic components as opposed to on top of some initial termination layer. The elimination of conventional initial termination layers (e.g., printed silver layers) as required in many prior art processes for effective adherence to the body of a terminated component and for providing a base to which additional termination layers may be plated offers a significant advantage. The elimination of such a base termination layer is enabled in part by the provision of exposed internal electrode elements or other conductive elements at specifically selected locations along the periphery of multilayer electronic components. By providing such exposed conductive portions in specifically defined and proximal locations, the formation of plated terminations directly on an electronic component (as opposed to on an initial adhesion termination layer) may be formed in a self-guided process.

Since all aspects set forth in clarified claim 1 as requested to be amended herewith are not disclosed in Maher et al., such reference cannot by law anticipate such clarified claim 1. Since claims 3-5 and 8-11 further limit presently clarified claim 1,

Maher et al. cannot by law anticipate claims 3-5 and 8-11, and acknowledgement of the same is earnestly solicited.

McLoughlin discloses a method for providing a nickel barrier end termination in which a zinc oxide semiconductor device is controllablly reacted with nickel plating solution only on an exposed end terminal region. Controllable contact of the component body and the nickel plating solution is required to assure that the nickel barrier end terminations 30 uniformly cover terminal region 32 without extending undesirably along exposed surface 38 (see col. 3, lines 47-52). The technology disclosed in McLoughlin is quite different from the termination technology set forth in presently clarified claim 1.

Claim 1 as requested to be amended herewith sets forth a clarified method of forming electrolessly plated structures for electronic components, including a step of fully immersing a plurality of electronic components in an electroless plating bath solution for a predetermined amount of time such that a plating material is deposited on selected of exposed internal electrodes of the plurality of electronic component, and so that a termination structure is developed by controlled bridging of the plating material among selected of the exposed internal electrode elements. Thus, the plating process set forth in presently clarified claim 1 results in plating determined by the location of the exposed electrode elements. In accordance with such clarified claim 1, the components are fully immersed as opposed to selectively dipped as disclosed in McLoughlin. The precision-controlled contact required in the methods of McLoughlin is a complicated and impractical procedure.

If the methodology set forth in McLoughlin were modified from controllable contact of a semiconductor device with the disclosed plating solution to complete or full immersion of such semiconductor devices, the plating would adhere to the entire surface of the device. **Such would destroy the device functionality** without the incorporation of additional process steps to then remove certain portions of the plated material. This is described as a prior art disadvantage in col. 1, lines 36-50 of McLoughlin and as a phenomena that is avoided in accordance with the simplified manufacturing process of McLoughlin. Thus, McLoughlin **teaches away from complete immersion** of electronic components in a plating solution to form selectively

deposited termination material. Applicants note that in accordance with §2141.03 of the MPEP, prior art must be considered in its entirety, including disclosures that teach away from the claims.

Since all steps set forth in presently clarified claim 1 are not disclosed in McLoughlin, specifically the steps of providing a plurality of electronic components and fully immersing the entire plurality of such electronic components in a bath solution, such reference cannot by law anticipate such claim 1. Since claims 3-5 and 8-11 further limit claim 1, McLoughlin cannot by law anticipate claims 3-5 and 8-11, and acknowledgement of the same is earnestly solicited. Furthermore, McLoughlin teaches **away** from the process set forth in presently clarified claim 1 and its dependent claims and as such should not be cited against such claims.

REJECTION OF ORIGINAL CLAIMS 1-20 (35 U.S.C. §103(A)):

Original claims 1-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,310,757 (Tuzuki et al.) in view of U.S. Patent No. 3,992,761 (McElroy et al.). Based on the following remarks, Applicants respectfully traverse such rejection and respectfully request reconsideration thereof.

Presently clarified independent claims 1 and 12 as requested to be amended herewith, set forth respective methods of forming electrolessly plated structures or terminations for electronic components, and both include a step of fully immersing a plurality of electronic components in an electroless plating bath solution for a predetermined amount of time such that a plating material is deposited on the plurality of electronic components to form respective bridged terminations or termination structure among selected of the exposed internal electrode elements. Both Tuzuki et al. and McElroy et al. references fail to disclose all such elements of presently clarified independent claims 1 and 12.

Tuzuki et al. discloses an electronic component with external electrodes and related process steps for forming such a component. The multi-layered external terminations formed in Tuzuki et al. include a first conductive layer 16 that is formed by preparing a conductive paste, dipping one end portion of each capacitor element into

the paste layer and drying the paste, then dipping another portion of the capacitor element in the paste layer and drying the paste. After applying the initial conductive layer 16, an optional palladium layer 18 may be formed as well as layers of electrolytically plated nickel 20b and solder 20a. There are many differences between the above terminations and related process steps as disclosed in Tuzuki et al. and the termination formation processes set forth in presently clarified claims 1 and 12.

Presently clarified claims 1 and 12 respectively set forth that the subject terminations or plated structures (which are formed by depositing plating material directly on the electronic components) are formed by fully immersing a plurality of electronic components in an electroless plating bath solution. In contrast, the initial conductive layer of the Tuzuki et al. terminations is formed by carefully dipping only the end portions of the capacitor chips in conductive paste. If such termination material were applied according to the process of presently clarified independent claims 1 and 12, the conductive paste would cover the entire ceramic body, shorting together all of the capacitor electrodes and destroying the functionality of the capacitors. Furthermore, the precision component dipping must be done twice per component on an individual component-by-component basis, not in a bulk process as set forth in presently clarified claims 1 and 12, whereby a plurality of electronic components are simultaneously terminated. The processes set forth in claims 1 and 12 are much more time efficient and cost effective than that disclosed in Tuzuki et al.

Thus, the application of the initial conductive layers 16 of Tuzuki et al. cannot be the same as the plating referred to in such claims 1 and 12. Furthermore, the electrolytic nickel and/or solder layers disclosed in Tuzuki et al. cannot be compared to the plating referred to in such claims 1 and 12. The electrolytic Ni layer 20b disclosed in Tuzuki et al. is not formed directly on the electronic components, but instead over the initial conductive layer or subsequently applied Palladium layer. A fundamental aspect of the process set forth in clarified claims 1 and 12 is that the subject plated terminations or plated structures are formed directly on the electronic components (a combination of ceramic substrate layers and exposed electrode portions) as opposed to on an initially-applied totally conductive surface. The elimination of conventional initial

termination layers (e.g., thick-film paste layers) as required in many prior art processes for effective adherence to the body of a terminated component and for providing a base to which additional termination layers may be plated offers a significant advantage. The elimination of such a base termination layer is enabled in part by the provision of exposed internal electrode elements or other conductive elements at specifically selected locations along the periphery of multilayer electronic components. By providing such exposed conductive portions in specifically defined and proximal locations, the formation of plated terminations directly on an electronic component that bridge between exposed internal electrode elements may be formed in a self-guided process. Plated terminations or structures that bridge between specifically oriented exposed conductive portions is not required or even desired in the plating processes of Tuzuki et al.

The USPTO position attempts to cure the deficiencies of Tuzuki et al. by citing McElroy et al. However, McElroy et al. is also fundamentally different from the termination methodology set forth in respective presently clarified claims 1 and 12. McElroy et al. discloses a step of forming electrically conductive termination films 18 on portions of an array of multi-layer capacitors. The termination films may correspond to an electrically conductive metal such as nickel or copper and may be formed in accordance with electroless plating techniques, but the way in which the resultant location of the termination films are defined and formed is quite different than in accordance with the methods of presently clarified claims 1 and 12.

Before the termination films 18 of McElroy et al. can be formed, a plurality of capacitors must be inserted through holes in a thin support sheet then encapsulated in a block of plastic material. The block is then immersed in a suitable solvent to dissolve or soften a given portion of the block such that exposed portions 19a of the outer surfaces 19 of each of the capacitor bodies 12 is exposed (see Fig. 8 and col. 3, line 61 – col. 4, line 34.) The exposed ends must then be immersed in an etchant to treat the exposed surfaces for improved adherence of subsequently applied termination films. The entire block must also be immersed in a sensitizing material before being subjected

to the plating material such that metal will only plate on the sensitized exposed surfaces of the capacitor bodies.

Claims 1 and 12 as presently clarified herewith set forth that the plurality of electronic components are fully immersed in an electroless plating bath solution and plating material bridges the exposed internal electrode elements to form terminations or plating structures directly on the electronic components. No additional steps such as providing an encapsulating block, sensitizing select exposed portions of the components, etc. is required as in the process disclosed in McElroy et al. In contrast, the location of the present plating material corresponds only to the location of the exposed internal electrodes. By providing exposed conductive portions in specifically defined and proximal locations, the formation of plated terminations or structures directly on an electronic component that bridge between exposed internal electrode elements may be formed in a self-guided process. Plated terminations or structures that bridge between specifically oriented exposed conductive portions is not required or even desired in the plating processes of McElroy et al.

Since all aspects set forth in presently clarified claims 1 and 12 are not disclosed singularly or in combination of the Tuzuki et al. and McElroy et al. references, such claims 1 and 12 should be allowed over such references. Also, since claims 2-11 and 13-20 variously depend from otherwise allowable respective independent claims 1 and 12 as presently requested to be amended herewith, and further limit same, claims 2-11 and 13-20 should also be allowed. Acknowledgement of the same is earnestly solicited.

REJECTION OF ORIGINAL CLAIMS 2, 6, 7 and 12-20 (35 U.S.C. §103(A)):

Original claims 2, 6, 7 and 12-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Maher et al. or McLoughlin in combination with Tuzuki et al. Based on the following remarks, Applicants respectfully traverse such rejection and respectfully request reconsideration of the rejected claims.

The previous remarks in the section of this paper regarding the rejection of original claims 1, 3-5 and 8-11 describe several fundamental differences between the steps set forth in presently clarified claim 1 as requested to be amended herewith and

the technologies disclosed in both Maher et al. and McLoughlin. The same differences also equally apply to the technology set forth in presently clarified independent claim 12, and Applicants refer to the same arguments for the 35 U.S.C. §103(a) rejection of claims 2, 6, 7 and 12-20. Also, the remarks in the immediately preceding section re the rejection of claims 1-20 distinguish the subject matter of presently clarified claims 1-20 from the disclosure of Tuzuki et al. and Applicants refer to those arguments as well for the subject rejection.

In general, presently clarified independent claims 1 and 12 set forth steps for terminating (i.e., plating) a plurality of components in a bulk process. A plurality of electronic components are provided with ceramic substrate layers and internal electrode elements selectively interleaved such that the internal electrode elements are exposed at predetermined locations along the periphery of the components. Full immersion of such plurality of electronic components in an electroless plating solution enables the formation of bridged terminations or plating structures based on the location of the exposed internal electrode elements. **This self-guided formation of component terminations or plated structures eliminates many complicated steps that are involved with prior art and other termination processes. There is no precision dipping of components in a termination paste or plating solution, no masking of components is required and the components do not need to be held in a certain way for the termination process of claim 1 to effectively occur. The plating material goes where the electrodes are exposed, thus yielding a unique self-determining termination process.**

In contrast with the above features as set forth in presently clarified claims 1 and 12, the technology disclosed in Maher et al. and in Tuzuki et al. both are directed to forming plated layers on top of a totally conductive surface where no bridging terminations among exposed conductive elements are required or even suggested. If modifications to such references were proposed to eliminate the initial conductive termination layer or to apply the subsequent termination layers directly to surfaces other than the totally conductive initial termination layers, the principles of operation of such

disclosed processes would be changed. In accordance with §2143.01 of the MPEP, proposed modifications cannot change the principle of operation of a reference.

The techniques disclosed in such references and also that disclosed in McLoughlin correspond to respective processes for forming external electrodes in often complicated and expensive procedures that require high levels of precision and individual component placement as opposed to the batch processing set forth in presently clarified claims 1 and 12 where a plurality of components are fully immersed in a plating solution. Furthermore, McLoughlin teaches away from complete immersion of electronic components in a plating solution (see col. 1, lines 36-50). As such, McLoughlin should not be cited against the subject claims.

Based on the aforementioned remarks, Applicant submit that presently clarified independent claims 1 and 12 are patentable over the Maher et al., McLoughlin and Tuzuki et al. references, and acknowledgement of the same is earnestly solicited. Further, since claims 2, 6 and 7 and 13-20 variously depend from otherwise allowable respective presently clarified independent claims 1 and 12 and further limit same, Applicants further submit that claims 2, 6, 7 and 13-20 should also be allowed over such references.

CONCLUSION:

Inasmuch as all outstanding issues have been addressed, it is respectfully submitted that the present application, including presently clarified claims 1-20 as requested to be amended herewith, is in complete condition for issuance of a formal Notice of Allowance upon entry of the presently requested amendments, and action to such effect is earnestly solicited.

The Examiner is invited to telephone the undersigned at his convenience should only minor issues remain after consideration of this response in order to permit early resolution of same.

Respectfully submitted,

DORITY & MANNING,
ATTORNEYS AT LAW, P.A.

Richard M. Moose

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Date

RICHARD M. MOOSE
Registration No. 31,226

P. O. Box 1449
Greenville, South Carolina 29602-1449

Telephone: (864) 271-1592
Facsimile: (864) 233-7342